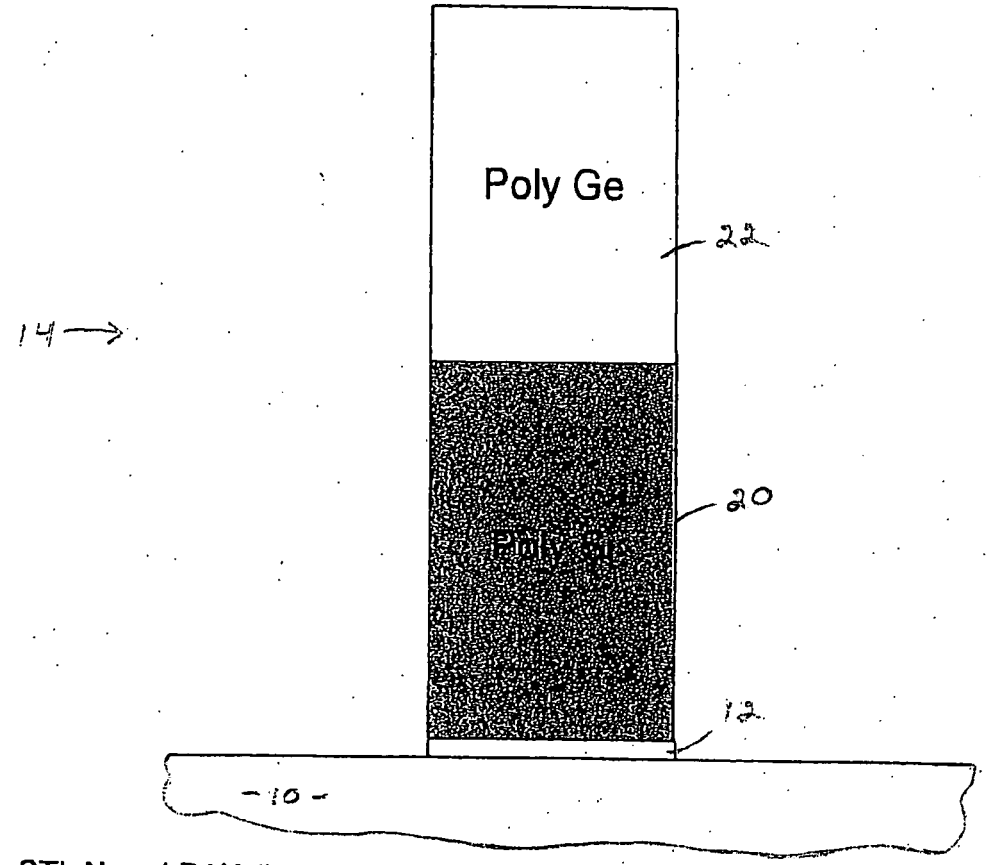
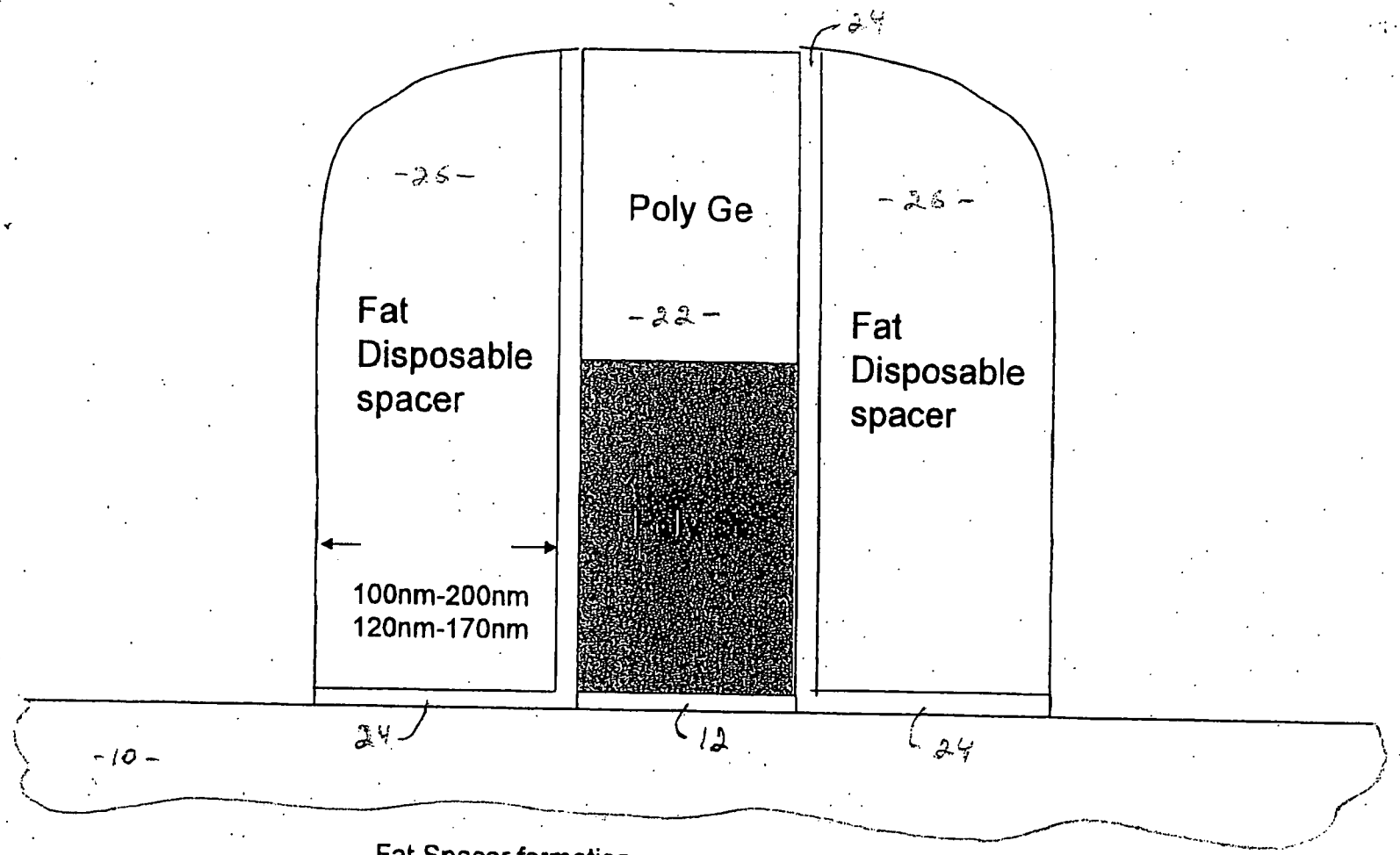


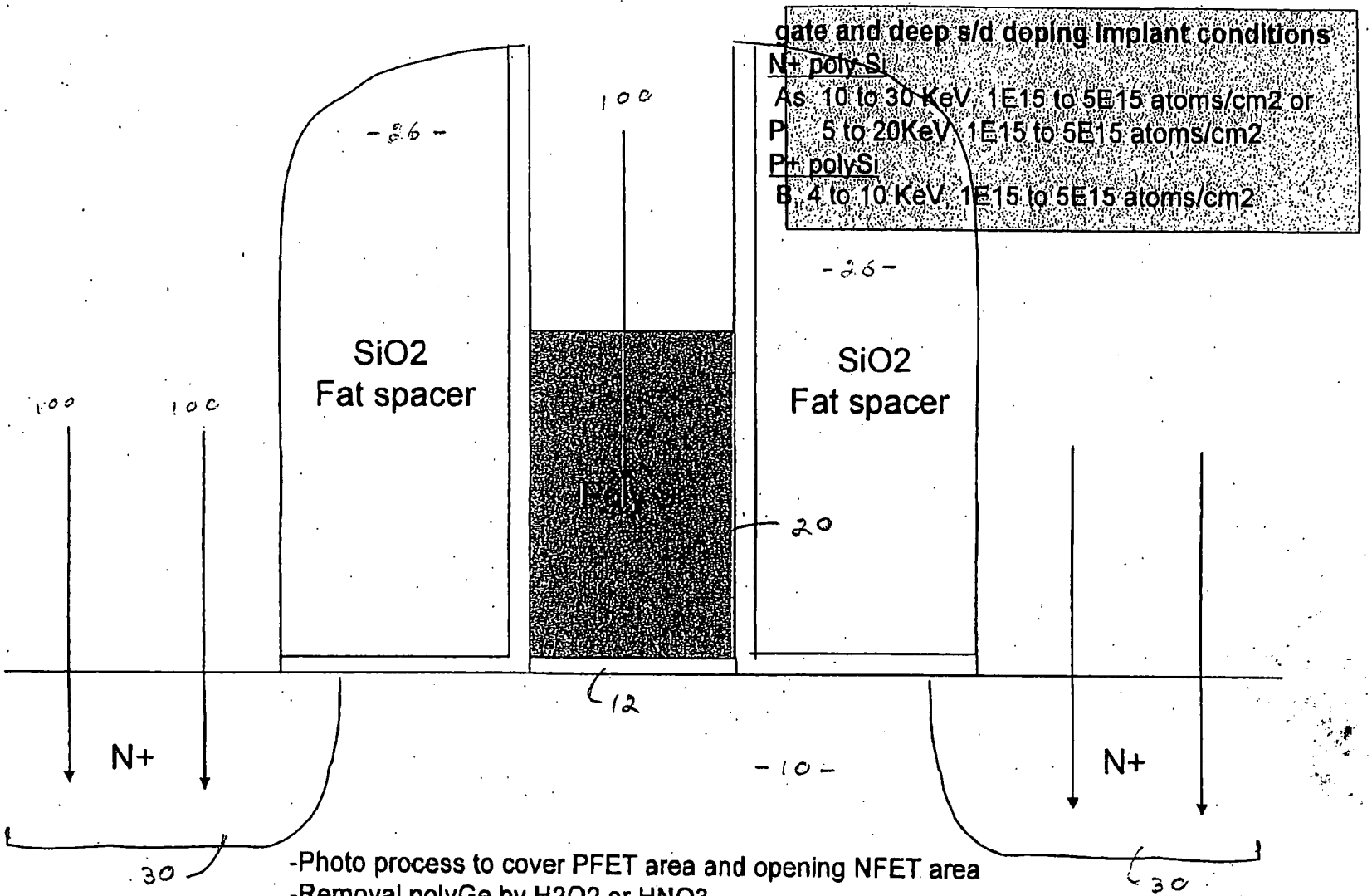
-STI, N and P Well,
-gate dielectric formation (plasma nitrided thermal oxidation or deposited oxynitride or nitride)
-Intrinsic polySi (~150nm) and intrinsic polyGe (~150nm) deposition
-Poly Si and PolyGe stack etch

Fig. 1



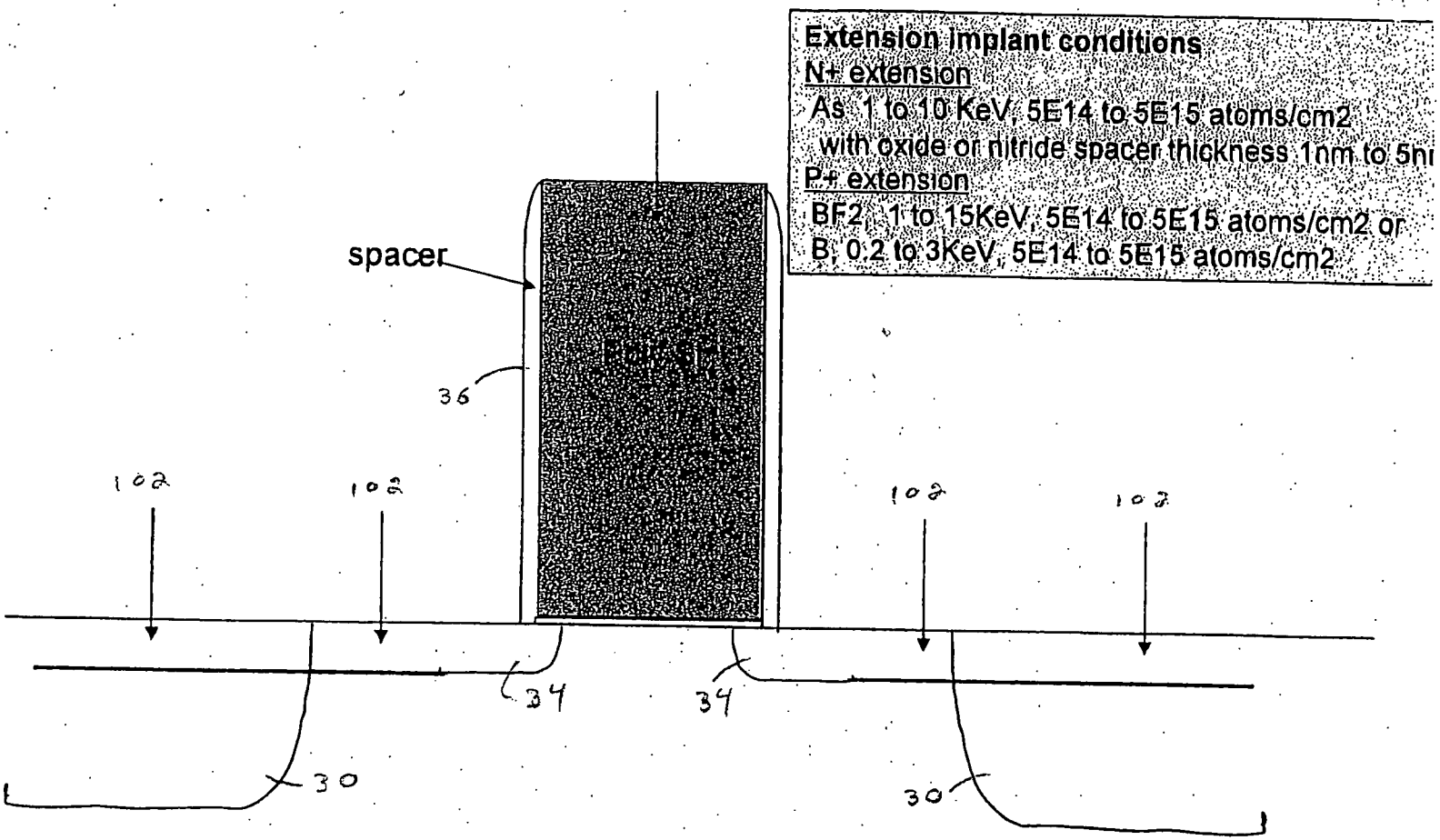
Fat Spacer formation
-Oxide/nitride liner deposition
- Conformal CVD or plasma CVD SiO2 deposition
- RIE directional etching of SiO2

Fig. 2



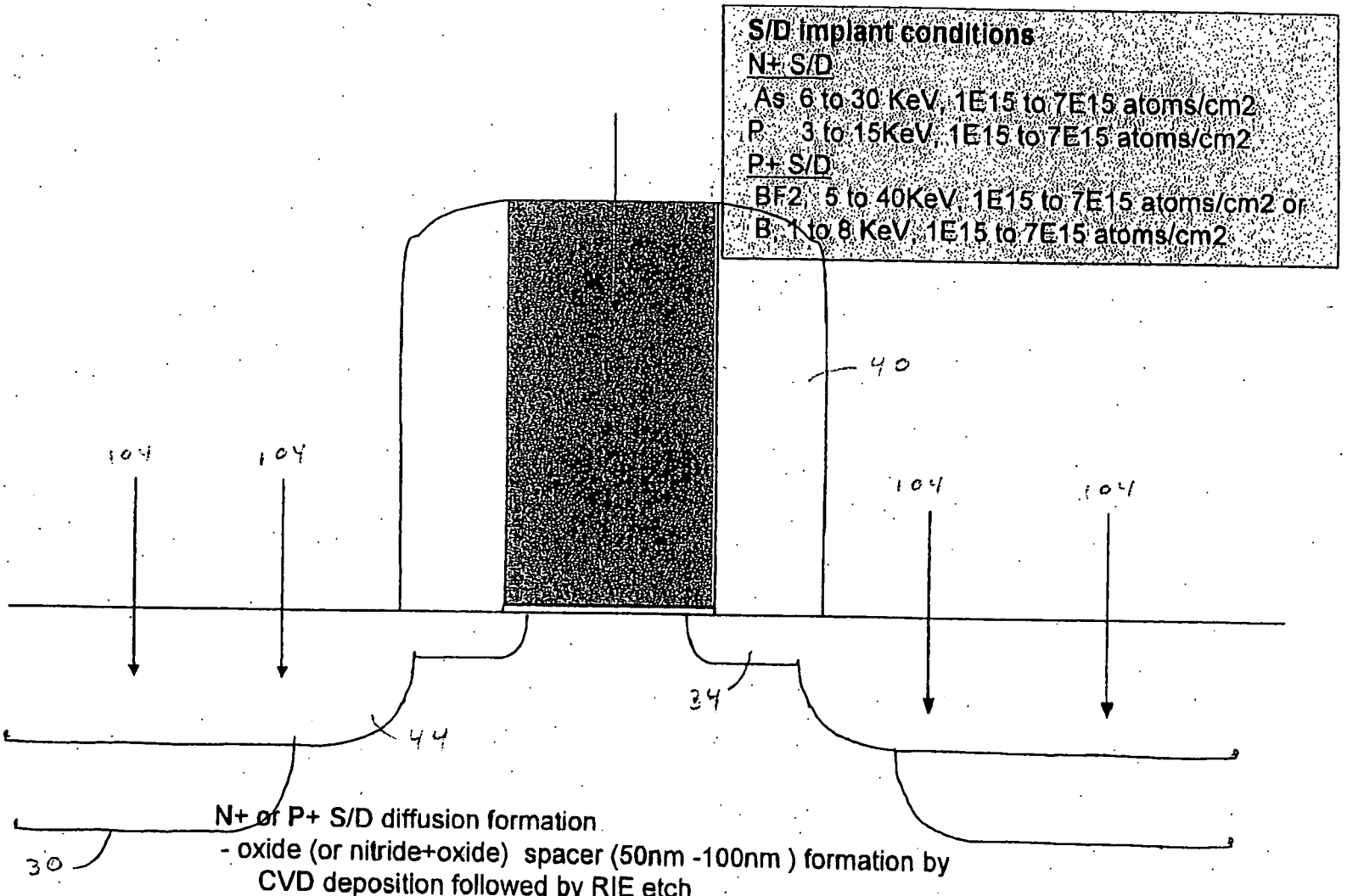
-Photo process to cover PFET area and opening NFET area
-Removal polyGe by H2O2 or HNO3
- As or P deep implant to dope poly Si and deep n+ s/d
-Photo process to cover NFET area and opening PFET area
-Removal of poly Ge by H2O2 or HNO3
-B deep implant to dope polySi and deep p+ s/d

Fig. 3



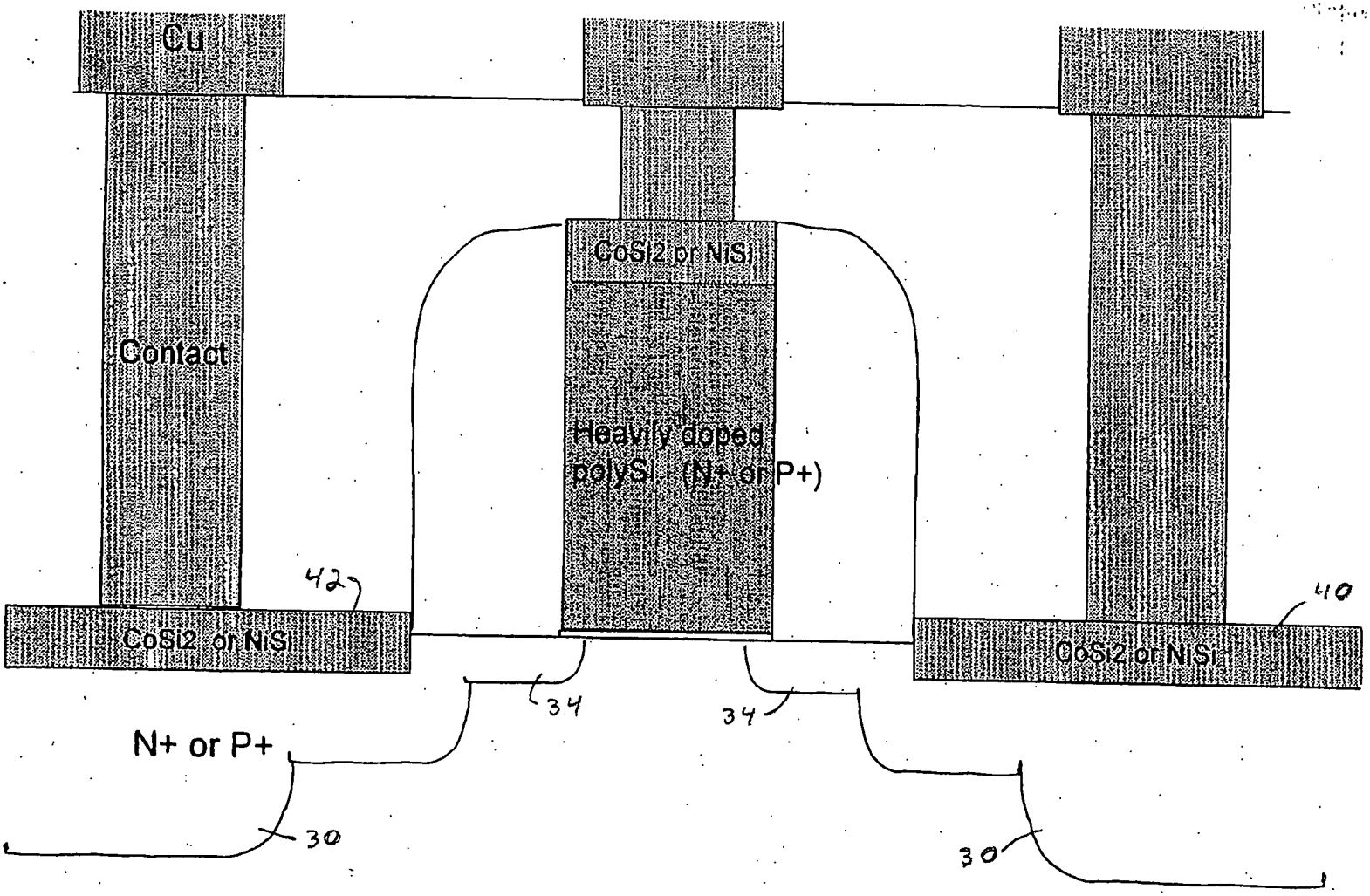
1. Removal of disposable spacer and liner
2. N+ or P+ extension formation
   - oxide or nitride spacer (less than 5nm for N, 15nm for P) formation by CVD deposition followed by RIE etch
   - As (for N) or B (for P) ion implantation, (halo implantations if necessary) with appropriate photo process to form implant blocking mask

Fig. 4



N+ or P+ S/D diffusion formation
- oxide (or nitride+oxide) spacer (50nm -100nm) formation by CVD deposition followed by RIE etch
- As or P (for N+) or B (for P+) ion implantation with appropriate photo process to form implant blocking mask,
- Strip photo resist after the implants
- Dopant activation anneal at 1000C to 1100C, for 10sec to 10m sec

Fig. 5



1. Silicide formation (CoSi2 or NiSi)
2. Device passivation insulator formation
   - CVD or PECVD of nitride and BPSG (Boronphosphrous Silicate) and planarization
3. Contact (W stud) and metal (Cu or Al) wiring formation

Fig. 6